Improving harmonic balance convergence behavior of nonlinear models

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***Abstract*— In this paper we demonstrate the influence of models non-linearities to harmonic balance simulation software, such as Agilents' ADS. Furthermore, we show how the large signal behavior in terms of convergence speed, time and region can be improved significantly. All methods proposed can be used for any kind of non-linear model, either analytical equations based or even table interpolated ones.**

Index terms **– non-linear modelling, harmonic balance, convergence, extrapolation**

I. Introduction

Under large signal conditions non-linear models often show convergence problems as soon as the device starts compressing. Sometimes, the harmonic balance algorithm needs a long time in order to converge, sometimes even no convergence can be reached at all due to several reasons.

The convergence behavior itself is influenced by several factors, such as

- number of internal nonlinear model nodes,
- interpolation function (equation based or table based),
- smoothness of interpolation function,
- smoothness and magnitude of describing functions derivatives,
- and extrapolation behavior.

To our experience, two points mentioned, extrapolation behavior and smoothness are the most critical parameters. While equation based mathematical functions, e.g. tanh-descriptions, are sufficiently smooth, spline interpolating function reproduce also measurement inaccuracies and spikes. In addition to that, spline functions only describe the measured or extracted region. An extrapolation has to be added as soon as the simulation leaves the measured range of bias points. Furthermore, spline functions use a certain order of polynomial terms, e.g. third order for cubic spline functions. Exceeding a low polynomial order may cause oscillations between measured and extracted element points especially when using very high orders.

II. Influence of interpolation function

Each nonlinear intrinsic transistor equivalent circuit element must be described by a function, which is able to interpolate between measured bias points. While parameter based equations [1] are rather smooth by nature, spline type of interpolation [2] follow each each measurement outlier. At the outlier points a high order of magnitude derivative is generated, which influences both convergence speed and behavior badly.

Thus, either measured s-parameters or extracted

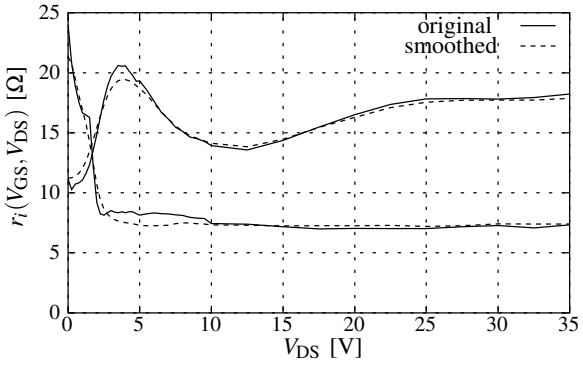

Fig. 1. Smoothed and extracted intrinsic resistor R_i for an LDMOS device.

intrinsic element values in dependence of the bias points should be smoothed as shown in fig. 1 for an intrinsic gate source resistor R_i. The grid has been smoothed using a simple $\cos^2$ FFT filtering [3] for both, V_{GS} and V_{DS} direction:

$$R_i(\rho) = \int_{-\infty}^{\infty} e(V_{GS}, V_{DS} = const.) e^{-j\rho V_{GS}} dV_{GS}. \quad (1)$$

After fourier transformation, the signal has been $\cos^2$ filtered and transformed back again.

Table I shows the computation time for a two-tone intermodulation simulation of an LDMOS device (-10 dBm ...+ 10 dBm step 0.5 dB RF power, $f = 2$ GHz, 100 kHz spacing, 10 harmonics). Despite of the total computation time it is obvious that harmonic balance

Extraction	non smoothed	medium smoothed	highly smoothed
Sim. time	48.26 s	38.12 s	36.57 s

TABLE I

HARMONIC BALANCE SIMULATION TIME.

within ADS converges quicker, the more smooth the extracted values are. A non-smoothed model converges 25% slower than a model based upon smoothed extraction data.

III. INFLUENCE OF EXTRAPOLATION

Furthermore, we want to demonstrate the influence of the extrapolation behavior to the nonlinear harmonic balance convergence performance. In doing so we use an TOPAS [3] LDMOS model and the Agilent ADS simulation software. Figure 2 shows an extracted gate source capacitance C_{gs} over the measured range of gate-source- and drain-source voltages. As can be seen, the extracted equivalent

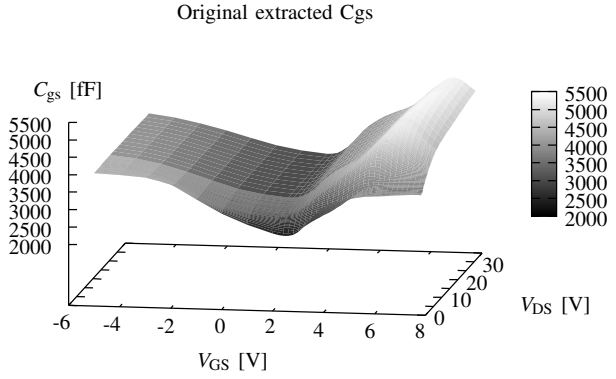

Fig. 2. Extracted gate-source capacitance C_{gs} for an LDMOS device.

circuit element C_{GS} shows a quite smooth shape. Nevertheless, during a harmonic balance simulation the circuit simulator often sets rather high and rather low voltage values in order to check the behavior of the intrinsic equivalent circuit elements at the boundaries and beyond. Fig. 3 shows a linear extrapolation of the extracted gate-source capacitance C_{GS}. The arrows mark extrapolation areas, which may cause convergence problems. In case of the extracted capacitance a linear extrapolation is not useable in order to fast and reliable achieve convergence behavior. Thus, we replaced the linear extrapolation for the used cubic spline interpolation by an tanh one. Instead of a linear extrapolation (here shown for the dimension one only)

$$y(x) = m\ x + b \tag{2}$$

the tanh expression

$$y(x) = m\ dx\ \tanh(x/dx) + b \tag{3}$$

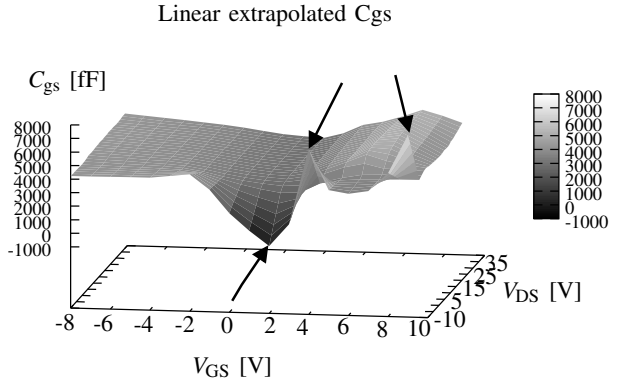

Fig. 3. Linear extrapolated gate-source capacitance C_{gs} for an LDMOS device. Arrows mark areas, which cause convergence problems during harmonic balance simulation.

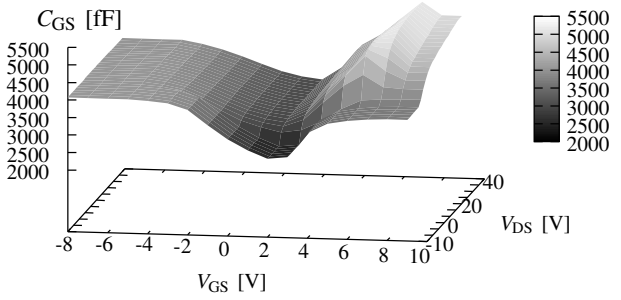

Fig. 4. Tanh-extrapolated gate-source capacitance C_{gs} for an LDMOS device.

is used, whereas m is the slope, b the y-axis intersection point and dx a convergence factor. During our experiments we detected values of dx in the range of $dx = 0.001 \ldots 0.1$ V. Nevertheless, in dependence of the simulation type (e.g. one tone or two tone harmonic balance) the optimum factor may vary, although the same transistor is used. Fig. 4 shows the extrapolated capacitance grid versus the bias voltages. As can be seen, this time the behavior is very smooth compared to linear extrapolation shown in fig. 3

IV. VERIFICATION RESULTS

In this section we show the influence of the extrapolation to one tone and two tone simulation results in comparison with measurements. All simulations have been carried out using Agilents' ADS circuit simulation software and the TOPAS LDMOS model [3, 4]. Fig. 5 shows a 2-tone intermodulation power sweep in comparison with measurements for a 3 finger 300 μm LDMOS device. The upper power sweep limit was set to maximum 60 dBm input power during simulation. Afterwards, we obtained

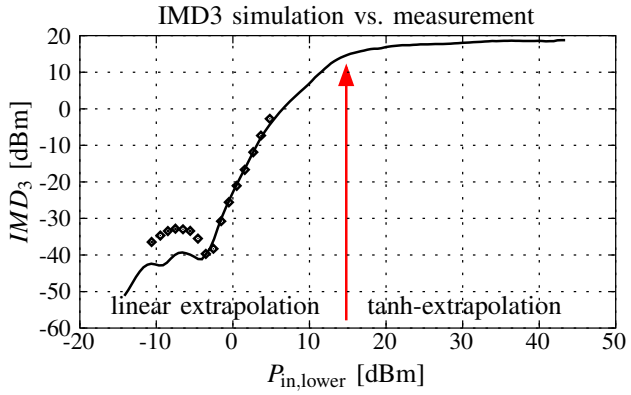

Fig. 5. Intermodulation simulation (line) versus measurement (dots) of a 3×300 μm LDMOS device at class B bias condition, $f = 2GHz$ and 100 kHz spacing. The arrow marks the convergence area for linear extrapolation (left site) and tanh extrapolation (right site). The model was scaled from a 7×300 μm LDMOS device.

the maximum input power the simulator could simulate without aborting the simulation due to convergence problems. The arrow marks the maximum input power the simulator handled using a linear extrapolation for the description of the bias dependent intrinsic elements (15 dBm). Using the proposed tanh type of extrapolation, the simulator simulated up to a maximum input power of 43 dBm without convergence problems. Thus, using the proposed method we could compress the device 28 dB more.

Similar examinations have been carried out for a 45 finger 300 μm LDMOS device (fig. 6). Also here the

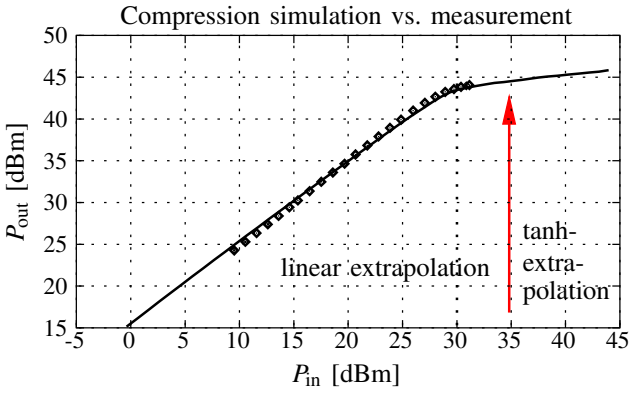

Fig. 6. Compression simulation (line) versus measurement (dots) of a 45×300 μm LDMOS device at class B bias condition, $f = 2$ GHz. The arrow marks the convergence area for linear extrapolation (left site) and tanh extrapolation (right site).The model was scaled from a 7×300 μm LDMOS device.

device could be compressed nearly 10 dB more using the proposed extrapolation method.

The simulation results themselves are not influenced by the extrapolation method.

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