A new precise large signal LDMOS(T) model including time delay effects

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***Abstract*— In this paper we present a new precise LDMOS(T) model. The model includes constant as well as bias dependent time delay effects. Furthermore, we demonstrate some new model extraction methods, which allow precise delay time calculations. The model has been implemented into Agilents' ADS[1] software. We show compression and intermodulation simulations in excellent comparison with measurements.**

I. LDMOS MODEL REQUIREMENTS

LDMOS transistor devices are often used for base station power amplifiers in class AB or B operation mode due to the required linearity. For this kind of applications LDMOS models must provide accurate compression and intermodulation behavior including higher order harmonics. This demand is fulfilled by a precise consistent small and large signal equivalent circuit [1] taking into account LDMOS related attributes such as a frequency dependent time delay or bias dependent isolation at the drain. Therefore, all bias dependent equivalent circuit elements must be described with high accuracy [2]. Furthermore, self heating and temperature effects must be modelled exactly. Nevertheless, in our work we neglected any temperature dependence caused by self heating effects due to the small device sizes we examined. These ventilations lead to the small signal equivalent circuitry presented in figure 1. For large signal operation all intrinsic capacitances are replaced with the current sources

$$i_{\mathrm{GS}} = c_{\mathrm{GS}}(V_{\mathrm{GS}},V_{\mathrm{DS}})\dot{V}_{\mathrm{GS}}, \quad (1)$$

$$i_{\mathrm{GD}} = c_{\mathrm{GD}}(V_{\mathrm{GS}},V_{\mathrm{DS}})\dot{V}_{\mathrm{GD}}, \quad (2)$$

$$i_{\mathrm{DS}} = c_{\mathrm{DS}}(V_{\mathrm{GS}},V_{\mathrm{DS}})\dot{V}_{\mathrm{DS}} \quad (3)$$

representing the large signal current caused by the charges on the capacitances c_{GS}, c_{GD} and c_{DS}. In this equivalent circuit the bias dependent drain resistor r_{D} describes the bias dependent drain isolation behavior and the low pass filter consisting of C_{if} and r_{if} the bias dependent delay time

$$\tau_{\mathrm{if}}(V_{\mathrm{GS}},V_{\mathrm{DS}}) = C_{\mathrm{if}}r_{\mathrm{if}}(V_{\mathrm{GS}},V_{\mathrm{DS}}). \quad (4)$$

This delay time is contrary to [3] bias dependent.

[1]ADS is a trademark of Agilent Technologies, CA.

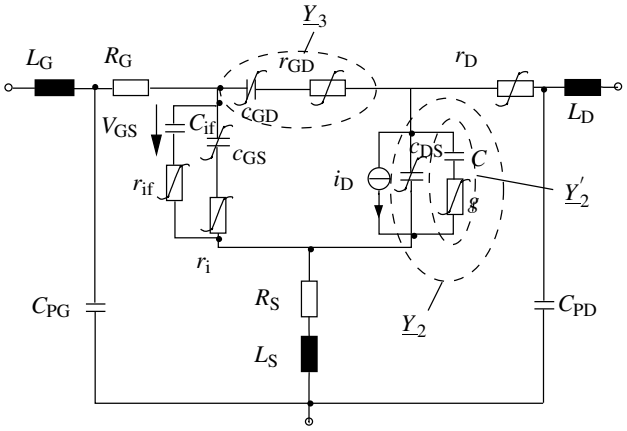

Fig. 1. Small signal LDMOS model equivalent circuit.

II. EXTRACTION STRATEGIES

The following section shows, how the LDMOS related extrinsic and intrinsic equivalent circuit elements can be extracted.

A. Extraction of the output conductance $g(V_{\mathrm{GS}},V_{\mathrm{DS}})$

As seen in figure 1, $\underline{Y}_3$ is defined as the serial branch consisting of c_{GD} and r_{GD}, $\underline{Y}_2$ represents c_{DS} in parallel with the series branch of C and g and $\underline{Y}'_2$ is the series branch of C and g itself. From the equivalent circuit follows with the measured $y_{22,\mathrm{meas}}$ parameter

$$y_{22,\mathrm{meas}} = \underline{Y}_2 + \underline{Y}_3 + \frac{\partial i_D}{\partial V_{\mathrm{DS}}}. \quad (5)$$

With

$$\underline{Z}'_2 = \frac{1}{\underline{Y}'_2} = \frac{1}{\mathrm{j}\omega C} + \frac{1}{g} \qquad \text{and} \qquad \underline{Y}_2 = \underline{Y}'_2 + \mathrm{j}\omega c_{\mathrm{DS}} \quad (6)$$

and

$$y_{22,\mathrm{meas}} - \underline{Y}_3 - \frac{\partial i_{\mathrm{D}}}{\partial V_{\mathrm{DS}}} - \mathrm{j}\omega C_{\mathrm{DS}} = \underline{Y}'_2 \quad (7)$$

follows

$$g = \frac{1}{\underline{Z}_2' - \frac{1}{\mathrm{j}\omega C}}. \tag{8}$$

B. The extraction of the time delay $\tau_{\mathrm{if}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$

The bias dependent time delay τ_{if} and therewith the frequency dependence of the current source can be calculated as follows. From the equivalent circuit follows within the small signal approximation

$$\begin{aligned} \underline{y}_{21,\mathrm{meas}} &= -\underline{Y}_3 + \frac{\partial i_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} \\ &= \Re e\{A\} + \mathrm{j}\Im m\{A\} \end{aligned} \tag{9}$$

with

$$\underline{Y}_3 = \frac{\omega C_{\mathrm{GD}}(\omega C_{\mathrm{GD}} R_{\mathrm{GD}} + \mathrm{j})}{1 + \omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}^2}. \tag{10}$$

Furthermore is

$$\begin{aligned} \frac{1}{Z} = \frac{\partial i_{\mathrm{D}}}{\partial V_{\mathrm{GS}}}(\omega) &= \frac{g_{\mathrm{m}}}{1 + \mathrm{j} r_{\mathrm{if}} C_{\mathrm{if}} \omega} \exp(-\mathrm{j}\omega\tau) \\ &= \frac{1}{\Re e\{Z\} + \mathrm{j}\Im m\{Z\}}. \end{aligned} \tag{11}$$

Solving this equation for r_{if} neglecting the phase factor yields

$$r_{\mathrm{if}} = \frac{\Im m\{Z\} g_{\mathrm{m}}}{\omega C_{\mathrm{if}}}. \tag{12}$$

Evaluating (9) and (11) with respect to the imaginary part results in $\Im m\{Z\}$, which can be written using the denominator

$$\begin{aligned} N &= \Re e^2\{A\}\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}^2 + \Im m^2\{A\}\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}^2 \\ &+ 2\Re e\{A\}\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}} + \omega^2 C_{\mathrm{GD}}^2 \\ &+ 2\Im m\{A\}\omega C_{\mathrm{GD}} + \Re e^2\{A\} + \Im m^2\{A\} \end{aligned} \tag{13}$$

as

$$\begin{aligned} \Im m\{Z\} &= (\cos(\omega\tau)\Im m\{A\} \\ &+ \cos(\omega\tau)\Im m\{A\}\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}^2 \\ &+ \cos(\omega\tau)\omega C_{\mathrm{GD}} + sin(\omega\tau)\Re e\{A\} \\ &+ sin(\omega\tau)\Re e\{A\}\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}^2 \\ &+ \sin(\omega\tau)\omega^2 C_{\mathrm{GD}}^2 R_{\mathrm{GD}}\big)/N \end{aligned} \tag{14}$$

with $A = \underline{y}_{21,\mathrm{meas}}$. Inserting this into (12) delivers r_{if} and using (4) τ_{if}. The constant value of C_{if} is chosen one order of magnitude below the smallest capacitance value in the equivalent circuit. In figure 2 a calculated τ_{if} for a 200 μm LDMOS device can be seen versus the bias voltages. For larger V_{DS} voltages and larger V_{GS} voltages the time delay raises as expected. The influence of this time delay can mainly be seen looking at the scattering parameter s_{21} (fig. 3). For frequencies above several GHz the simulation without taking τ_{if} into account (dash dotted line) predicts much more gain than the measurement

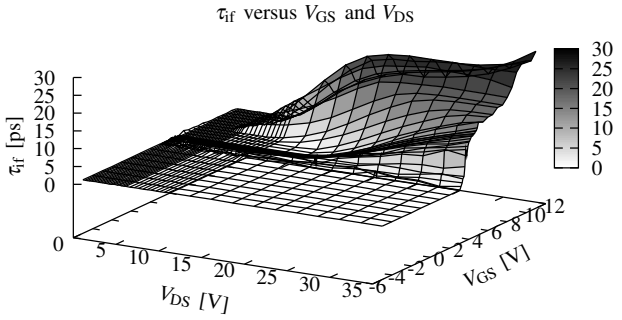

Fig. 2. Calculated τ_{if} for a 200 μm LDMOS device.

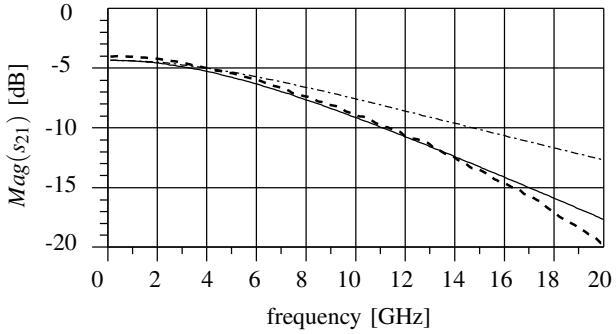

Fig. 3. Measured scattering parameter s_{21} (points) versus simulation with (line) and without (dashed dotted line) taking τ_{if} into account at class A bias condition for a 200 μm LDMOS device.

(points) or the simulation considering τ_{if} (line). Therefore, a bias dependent delay time τ_{if} is essential for any LDMOS model especially for the prediction of higher harmonics. Nevertheless, in many models used today [4, 5] showing just reasonable harmonic prediction, τ_{if} is ignored. All other extrinsic and intrinsic elements can be extracted as described in [6].

C. The extraction of the bias dependent drain resistor $r_{\mathrm{D}}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$

The bias dependent extrinsic drain resistor can hardly be extracted using an analytical approach. Thus, the optimizing process shown in fig. 4 is used for determining the bias dependence of the drain resistor r_{D}. Although optimization techniques are used, the result is a very smooth shape as can be seen in fig. (5) considering the r_{D} of a 200 μm device as an example. During the optimization process particular weighting has been set to the scattering parameters s_{11} and s_{22}. As can be seen the element behaves as expected. For lower V_{DS} voltage the LDMOS has a higher isolation and features therewith a higher drain resistance.

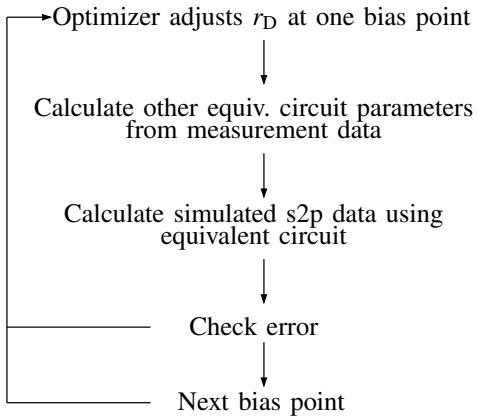

Fig. 4. LDMOS r_D extraction schema using optimization techniques.

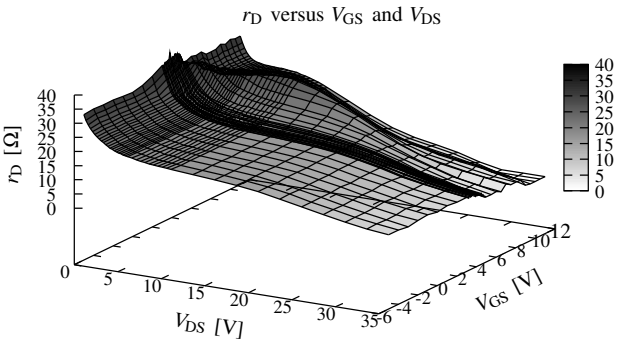

Fig. 5. Extracted extrinsic bias dependent drain resistor r_D for a 200 μm LDMOS device.

D. Smoothing

The proposed LDMOS model uses a precise bicubic spline interpolated table based approach

$$f(V_{GS},V_{DS}) = \sum_{j=1}^{4}\sum_{k=1}^{4} c_{jk} t^{j-1} u^{k-1} \tag{15}$$

with the spline coefficients c_{jk} and

$$t = \frac{V_{GS} - V_{GS,table}[j]}{V_{GS,table}[j+1] - V_{GS,table}[j]} \tag{16}$$

$$u = \frac{V_{DS} - V_{DS,table}[k]}{V_{DS,table}[k+1] - V_{DS,table}[k]} \tag{17}$$

whereby j and k represent the V_{GS} and the V_{DS} direction of the discrete measured element grids. The spline function is linearly extrapolated. Although bicubic spline functions do not intend to oscillate between measured points, smooth element shapes versus the bias voltage grids are required for a fast harmonic balance convergence. Therefore, and to average out any measurement and extraction inaccuracies, a data smoothing algorithm has been implemented using the fast fourier transformation (FFT)

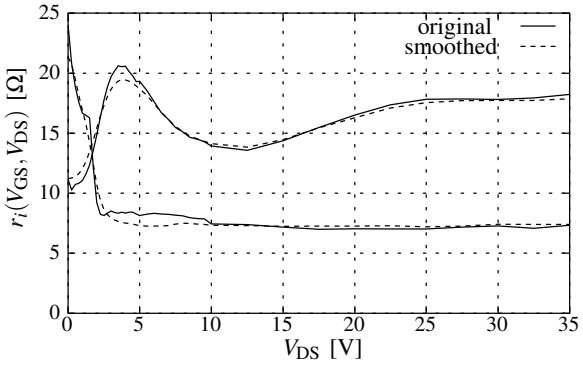

Fig. 6. Original extracted and smoothed values of the intrinsic r_i resistor of a 200 μm LDMOS device. Lower curve is for $V_{GS} = 4$ V, upper curve for $V_{GS} = 7$ V.

$$H(\rho) = \int_{-\infty}^{\infty} h(t) e^{-j\rho x} dx. \tag{18}$$

At first, for an intrinsic element $e(V_{GS},V_{DS})$ the FFT is calculated for constant values of V_{DS}:

$$E(\rho) = \int_{-\infty}^{\infty} e(V_{GS}, V_{DS} = const.) e^{-j\rho V_{GS}} dV_{GS}. \tag{19}$$

The result $E(\rho)$ is passed through a $\cos^2$ filter and transformed back. Afterwards, the same procedure is repeated for constant V_{GS} and changing V_{DS} values. Figure 6 demonstrates this algorithm for the intrinsic r_i resistor for the V_{GS} voltages 4 V (lower curve) and 7 V (upper curve).

III. Comparisons

In this section nonlinear measurements such as compression and intermodulation curves are compared with simulated results. Also higher harmonics have been evaluated. Figure 7 shows the simulated compression drain current I_D in excellent agreement with the measurement. The

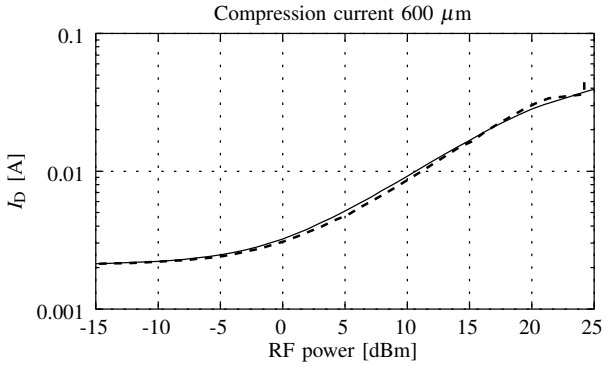

Fig. 7. Simulated (line) and measured (points) drain current I_D of a 600 μm LDMOS device at class B bias conditions and $f = 2.1$ GHz.

input power has been swept from $P_{in} = -15$ dBm to $P_{in} = 25$ dBm at a frequency of $f = 2.1$ GHz under class

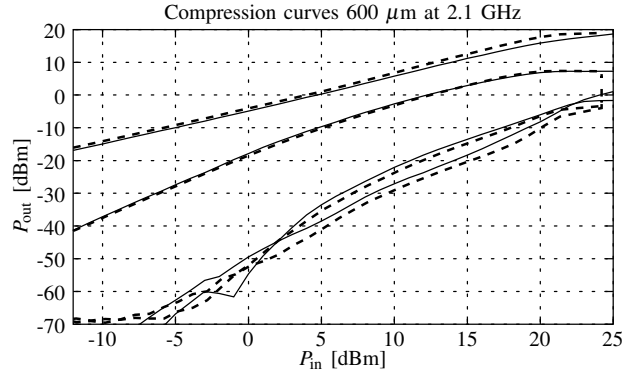

Fig. 8. Measured (points) and simulated (lines) compression behaviour of fundamental wave and higher harmonics (H0-H3) for a 600 μm LDMOS device at class B bias conditions and $f = 2.1$ GHz.

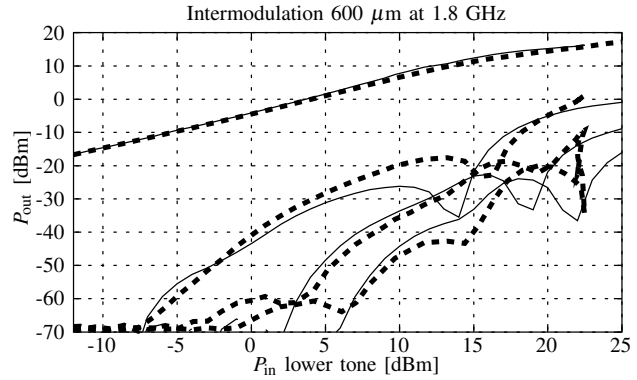

Fig. 9. Intermodulation measurement (points) versus simulation (lines) for a 600 μm LDMOS device at class B bias conditions and $f = 1.8$ GHz.

B bias conditions in an 50 Ω environment. Despite of the logarithmic scale, no differences between simulation and measurement can be obtained. Even the reversal point is modelled correctly. In fig. 8 the compression behavior of the fundamental wave and the higher harmonics can be seen in dependence of the input power. Bias setting and frequency are identical to fig. 7. It is obvious that the generation of harmonics and their behavior is described accurately, although the device is operated in pinch-off (class B mode) and is therefore very sensitive to slight bias voltage changes. In figure 9 intermodulation results are shown. The input power P_{in} is the power of the lower tone. The lower limit of the measurement system is - 70 dBm, the upper approximately 22 dBm. Thru measurements have been used for calibration. The last figure 10 shows the power added efficiency (PAE) versus the available input power $P_{\text{in,av}}$ for a 600 μm LDMOS device at class B bias condition (4.5 V/ 26 V) at a frequency of $f = 2$ GHz. The device has been matched at the output close to the optimum load impedance. Also under this matching condition, a very good agreement between measurement

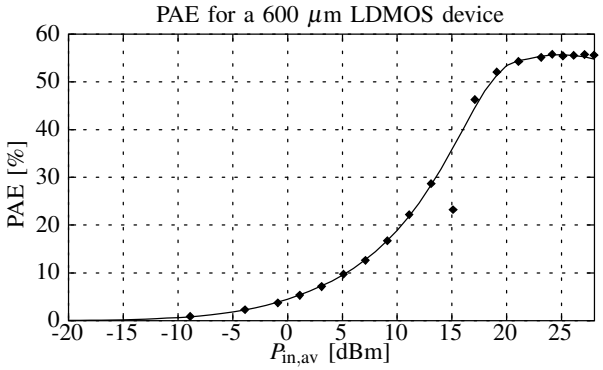

Fig. 10. Measured and simulated PAE of a 600 μm LDMOS device at matched class B bias conditions and $f = 2.0$ GHz. The output load impedance for the fundamental wave was $(150 + \text{j}230)\Omega$.

and simulation has been obtained.

IV. ACKNOWLEDGEMENT

We like to thank our colleagues of Philips Semiconductors in Nijmegen, Netherlands for the good cooperation and the on-wafer LDMOS devices provided. The next working steps scheduled are implementing self heating and environmental temperature effects as well as precise scaling options.

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