Consistent large signal implementation of capacitances driven by two steering voltages for FET modeling

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***Abstract*— In this paper we discuss the large signal behavior of capacitances extracted using small signal s-parameter measurements. We demonstrate under which conditions charge conservation is not preserved. In many models capacitances depending on two bias voltages are implemented as current sources under large signal conditions. We show an example, where a DC current flows through the mentioned kind of capacitance. Furthermore, we present a simple equivalent circuit solution in order to prevent any DC current to flow through capacitances.**

I. Large signal behavior of capacitances

The charge on a capacitor driven by only one steering voltage can be described as

$$Q(V_1) = \int_0^{V_1} C(\tilde{V}_1) d\tilde{V}_1. \tag{1}$$

This equation implicates charge conservation:

$$\Delta Q = \oint_{\Omega} C(\tilde{V}_1) d\tilde{V}_1 = 0, \tag{2}$$

if an analytical function $C(V_1)$ can be found and integrated. Nevertheless, the integration of a capacitance depending on two bias voltages is path dependent:

$$Q(V_1, V_2) = \int_0^{V_1, V_2} C(\tilde{V}_1, V_2) d\tilde{V}_1 + Q(V_2), \tag{3}$$

which may cause some problems in preserving the charge.

In practice, mainly small signal capacitances based on s-parameter measurements are extracted. These are integrated into circuit simulation software either as charge or current sources for large signal modelling purposes.

In the charge source case, charge conservation only can be guaranteed by calculating the small signal capacitances using a known charge equation formulation.

If the total charge under the transistor gate is

$$Q_g = aV_{GS}^2 + bV_{gs}V_{gd} + cV_{gd}^2, \tag{4}$$

the total gate current will be

$$i_g = \frac{\partial Q_g}{\partial V_{gs}} \frac{dV_{gs}}{dt} + \frac{\partial Q_g}{\partial V_{gd}} \frac{dV_{gd}}{dt}. \tag{5}$$

Assuming $V_{gs} = e\sin(\omega t)$ and $V_{gd} = f\cos(\omega t)$ (e and f are constants with unit volt) yields with (5)

$$i_g = \omega(A\sin(2\omega t) + B\sin(2\omega t)), \tag{6}$$

whereas ω is the radian frequency and $A = ae^2 - cf^2$ and $B = bef$. As can be seen the total gate current is purely capacitive and does not have any DC component.

However, if only extracted small signal capacitances are taken into account, these will be physically defined [1] as e.g.

$$C_{gs}(V_{gs}, V_{gd}) = \left.\frac{\partial Q_G}{\partial V_{gs}}\right|_{V_{gd}=const.} = 2aV_{gs} + bV_{gd}. \tag{7}$$

This results in a gate source part of the total gate current $i_g = i_{gs} + i_{gd}$ equal to

$$i_{gs} = \omega(E + D\sin(2\omega t) + E\cos(2\omega t)), \tag{8}$$

with $E = 0.5bef$ and $D = ae^2$, where ωE is an un-physical DC current component making the model unusable in practical applications.

This DC current phenomenon also can be observed on a capacitor $C(V)$ depending on one bias voltage V only. If the voltage V across the capacitors terminal consists on a small and a large amplitude V_0 and V_1, the current I through that capacitor can be defined as

$$I = C\frac{dV}{dt} = I_0 + I_1, \tag{9}$$

whereas I_0 and I_1 are small and large amplitude current parts. Linearizing C yields

$$C \approx C_0 + \frac{\partial C_0}{\partial V} V_1. \tag{10}$$

Inserting this C in equation (9) and eliminating the second order terms yields

$$C_0 \frac{dV_1}{dt} + \left(\frac{\partial C_0}{\partial V}\frac{dV_0}{dt}\right) V_1 = I_1. \tag{11}$$

The factor

$$\frac{\partial C_0}{\partial V}\frac{dV_0}{dt} = G(t) \tag{12}$$

describes a conductance, which allows a DC current through the capacitor C. Here, the step producing unphysical results is neglecting of $\partial C/\partial t$ in (9).

Correctly, the current I must be described as

$$I = \left(\frac{d(CV)}{dt}\right) = \frac{dC}{dt}V + \frac{dV}{dt}C. \tag{13}$$

Inserting the linearisation (10) in equation (13) yields

$$\left(C_0 + \frac{\partial C_0}{\partial V}V_1\right)(V_0 + V1) = \int I_0 dt + \int I_1 dt. \tag{14}$$

Eliminating second order terms again results in an effective pure capacitor C_{eff}, which can be denoted as

$$C_{\text{eff}}V_1 = I_1, \tag{15}$$

with

$$C_{\text{eff}} = C_0 + \frac{\partial C_0}{\partial V}V_0. \tag{16}$$

These considerations illustrate the importance of correct capacitance extraction using e.g. small signal measurements only. Furthermore, the transformation of these small signal capacitances into a nonlinear model may cause problems with respect to charge conservation.

II. Implementation into nonlinear circuit simulators

There are several ways of how nonlinear capacitances can be implemented into nonlinear circuit simulation software. Either, analytical charge equations are used or different methods such as transcapacitances [2] in order to preserve charge conservation. Nevertheless, in many cases small signal extracted capacitances in dependence of two bias voltages are simply replaced by a current source description as shown in equation (5) and (7). This implementation often is used in table based models. But it may result in an un-physical behavior such as a flow of gate current within a MOS device. When using the TOPAS [3] model for an LDMOS device, this fact could be obtained for large input power as demonstrated in figure 1. The figure shows the gate current during an intermodulation simulation. As clearly can be seen, the simulated gate current rises with rising input power up to 2 mA, whereas the measured one stays at 0 mA. The simulated behavior is not physical, simply because there exists no current through the gate oxide of an LDMOS transistor device. It is caused by the non charge conserving implementation of large signal capacitances driven by two bias voltages. Furthermore, the effect rises with rising input power and can not be seen under small signal conditions.

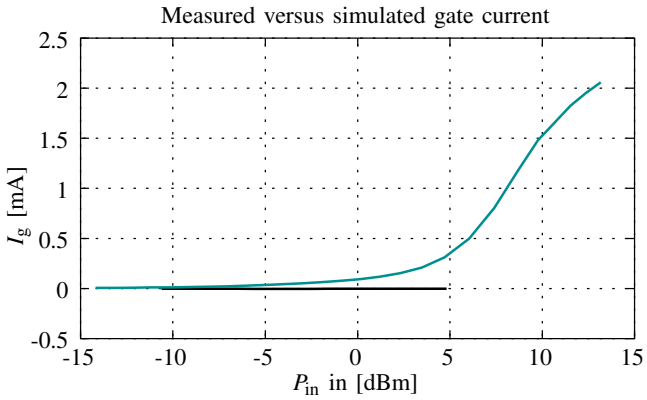

Fig. 1. Measured (lower curve) and simulated (upper curve) gate current versus input power for a $3 \times 300\mu m$ LDMOS device.

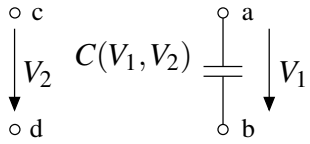

Fig. 2. Small signal capacitance depending on two bias voltages V_1 and V_2.

III. Forced charge conservation

Charge conservation can be forced by replacing small signal capacitances driven by two bias voltages (fig. 2) with the construction shown in figure 3. Any DC current component arising from the violation of the charge conservation is blocked by the constant capacitor C. Nevertheless, if a DC current is generated, harmonic balance calculation behavior of the circuit simulator will be influenced badly. Thus, the inductor in parallel to the current source allows DC current flow without disturbing the circuit.

In this way, charge conservation is forced using equivalent circuit elements. The values of C and L should be quite larger in order to not disturb the characteristics of the remaining equivalent circuit.
When using the construction shown above, any gate current is prohibited as can be seen in the next figure. Should a real gate current be simulated e.g. for JFET or MESFET devices, a diode can be connected between terminal a and b (fig. 3).
The convergence behavior is not influenced by these additional two linear elements.

IV. Verification results

In this section we want to demonstrate the good performance, which can be achieved replacing the small

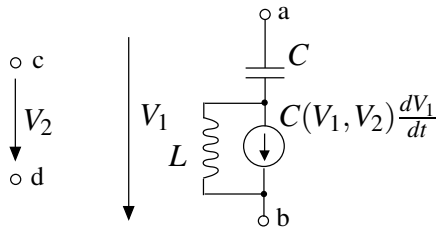

Fig. 3. Large signal implementation of a capacitor driven by two voltages V_1 and V_2.

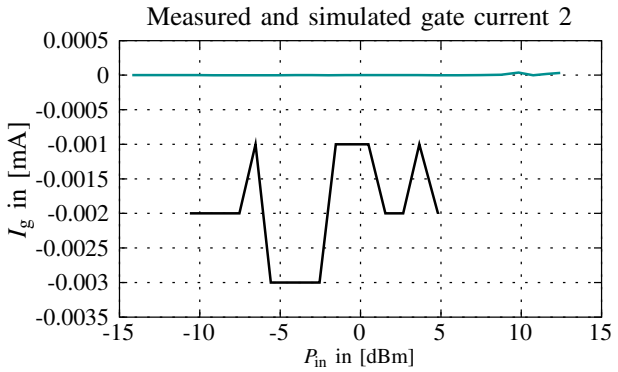

Fig. 4. Measured and simulated gate current after charge conservating implementation of current source.

signal capacitors with large signal current sources as described above. The verification shows an intermodulation measurement versus a simulation (IMD3) for a 3 finger 300 μm LDMOS device. This device was simulated using a scaled 7 finger 300 μm model. Operation is at class B bias condition, a frequency of 2 GHz and an offset frequency of 100 KHz. Although the bias configuration

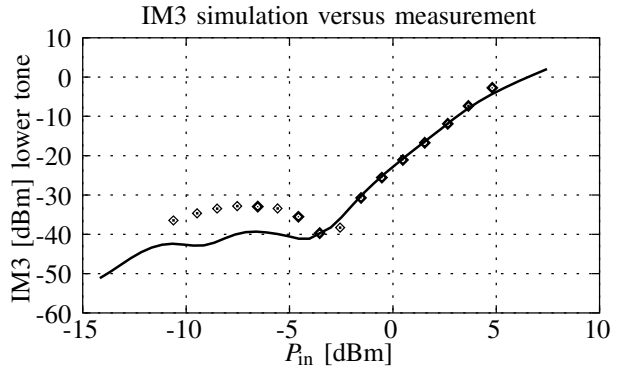

Fig. 5. Measured (dots) and simulated (line) intermodulation results (IM3, lower tone) at class B bias conditions, 2 GHz center frequency and 100 KHz offset frequency.

is quite critical for intermodulation type of simulation and model was scaled, the simulation is in good agreement with measurement results. Simulation results based on a wrong implemented current source are nearly identical to the results shown above.

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