Precise simulation of LDMOS temperature effects using tricubic spline functions

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Abstract—**Power transistor devices such as LDMOS change their behavior during operation due to self heating effects. This effect is often described using functional descriptions [1] for the IV output characteristics. In this paper we show the limits of this approach. Furthermore, we present an efficient extraction and simulation method describing self-heating based on tricubic spline functions.**

I. Thermal model

Most transistor models use the well-known parallel circuitry consisting of a thermal resistance R_{TH} and a thermal capacitance C_{TH} in serial with the voltage source (fig. 1) representing the ambient temperature for the simulation of self-heating effects. This thermal

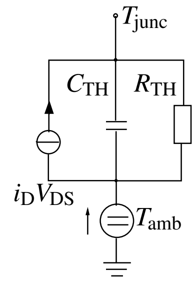

Fig. 1. Thermal equivalent circuit.

equivalent circuit (fig. 1) solves the heat transportation equation

$$C_{\mathrm{TH}}\frac{d\Delta T}{dt} = I_{\mathrm{D}}V_{\mathrm{DS}} - \frac{\Delta T}{R_{\mathrm{TH}}}, \qquad (1)$$

whereas ΔT is the difference between ambient T_{amb} and junction temperature T_{junc} and $I_{\mathrm{D}}V_{\mathrm{DS}}$ the DC power loss. During simulation this differential equation is solved. The delivered junction temperature is than used to steer the drain current source in most transistor equivalent circuits. Although the MET (Motorola's Electrothermal LDMOS Model) drain current equation [1] uses over 20 parameters, the simulation accuracy in comparison to measurements was rather poor for the examined LDMOS devices. Figure 2 shows that agreement between simulated and measured isothermal IV-curves.

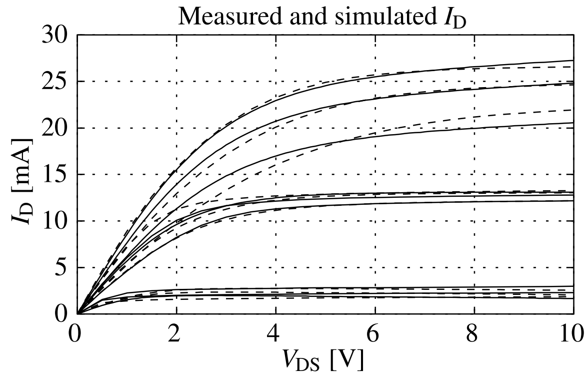

Fig. 2. Measured and simulated iso-thermal IV curves using the MET model at 25 °C, 75 °C and 100 °C at $V_{\mathrm{GS}} = 5, 7, 9$ V.

II. "Tricubic" spline functions

In order to avoid high optimization times and to achieve a perfect agreement between measurement and simulation we introduced tricubic spline functions. These functions reproduce a bias and temperature dependent drain current source $I_{\mathrm{D}}(V_{\mathrm{GS}}, V_{\mathrm{DS}}, T)$ with the highest possible accuracy. The spline function itself is defined as

$$f(\vec{x}) = \sum_{i=0}^{3}\sum_{j=0}^{3}\sum_{k=0}^{3} a_{ijk}x_1^i x_2^j x_3^k. \qquad (2)$$

This equation delivers 64 unknown values per interpolation point, which can be solved using the continuity conditions for f, $\frac{\partial f}{\partial x_i}$, $\left.\frac{\partial^2 f}{\partial x_i \partial x_j}\right|_{i \neq j}$ and $\frac{\partial^3 f}{\partial x_1 \partial x_2 \partial x_3}$ for 8 points at a time. The calculation of these spline coefficients does not require any optimization process and is generally applicable to any functional interrelationship $I_{\mathrm{D}}(V_{\mathrm{GS}}, V_{\mathrm{DS}}, T)$. Using the continuity conditions the proposed spline function is linearly extrapolated.

III. Thermal resistance extraction methods

For thermal resistance extraction one continuous at a fixed ambient temperature and several iso-thermal IV output characteristic measurements at different ambient temperatures have been taken into account. In opposite to [2] a rather simple extraction procedure was used. For each bias point V_{GS} and V_{DS} the drain current continuous I_{D} is stored at the fixed ambient temperature T_{amb}. Afterwards, the temperature $T_{\mathrm{amb}} \approx T_{\mathrm{junc}}$ of iso-thermal drain current at the same bias conditions is varied, until both currents are identical. This is done in a simple optimization loop. If both currents are identical, the dc power loss is known and therewith the thermal resistance

$$R_{\mathrm{TH}} = \frac{T_{\mathrm{junc}} - T_{\mathrm{amb}}}{I_{\mathrm{D}} V_{\mathrm{DS}}}. \qquad (3)$$

For verification purpose simulation data have been used. First, simulated iso-thermal IV curves at different temperatures have been calculated using a $R_{\mathrm{TH}} = 0.1\ ^\circ\mathrm{C/W}$. Afterwards, the thermal resistance was set to $R_{\mathrm{TH}} = 30.0\ ^\circ\mathrm{C/W}$ and a simulation was performed at a certain ambient temperature. Fig. 3 shows the extraction result. As can be seen R_{TH} shows the expected value.

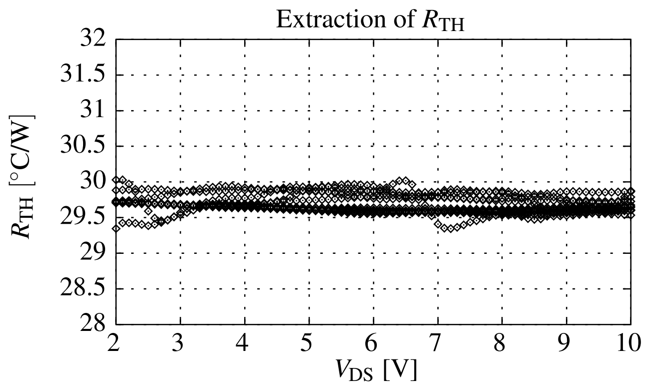

Fig. 3. Extraction of R_{TH} using simulated iso-thermal IV-curves at different temperatures and one continuous IV-curve. The gate-source voltage was varied from 5 to 15 V.

This procedure will also work for IV curves measured at different constant ambient temperature and just one pulsed IV curve at a rather high ambient temperature. Furthermore, the thermal resistor can be extracted without using any pulsed measurements. Taking CW IV curves at different ambient temperatures into account, the pulsed behavior of these curves can be calculated by estimating and varying a curtain thermal resistor value, until the linear inter- and extrapolation $I_{\mathrm{D}}(V_{\mathrm{GS}}, V_{\mathrm{DS}}, T_{\mathrm{amb}})$ towards $I_{\mathrm{D}}(V_{\mathrm{GS}}, V_{\mathrm{DS}}, T_{\mathrm{junc}})$ shows zero slope in the saturation region. Fig. 4 has been carried out for a $7\times100\ \mu$m LDMOS device. The agreement has been reached using a value of R_{TH} = 60 K/W. The thermal capacitance can be extracted using the current signal versus time within a pulsed measurement setup.

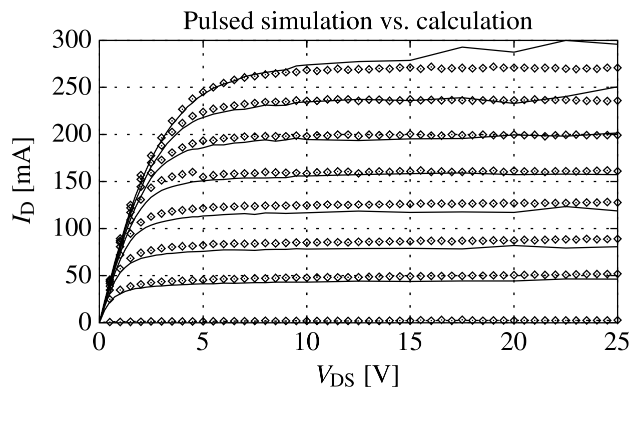

Fig. 4. Extraction of R_{TH} using measured pulsed curves and calculated IV curves transformed from constant ambient temperature towards constant junction temperature.

IV. Verification results

A. Isothermal verification

The proposed tricubic spline approach has been implemented into the TOPAS [3] model. Figure 5 shows the same measurement versus simulation as figure 2, but this time using the TOPAS model. As can be seen, there are absolutely no differences between measured and simulated iso-thermal IV-curves. The next figure shows the iso-thermal transfer characteristic for the 200 μm LDMOS device. Also here, absolutely no differences between measurement and simulation can be obtained. Furthermore, all curves intersect in one point as expected.

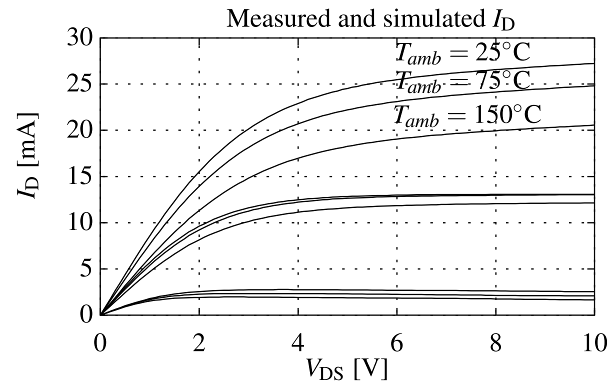

Fig. 5. Measured and simulated iso-thermal IV curves using the TOPAS model at 25 °C, 75 °C and 100 °C at $V_{\mathrm{GS}} = 5, 7, 9$ V. Simulation and measurement curves are identical.

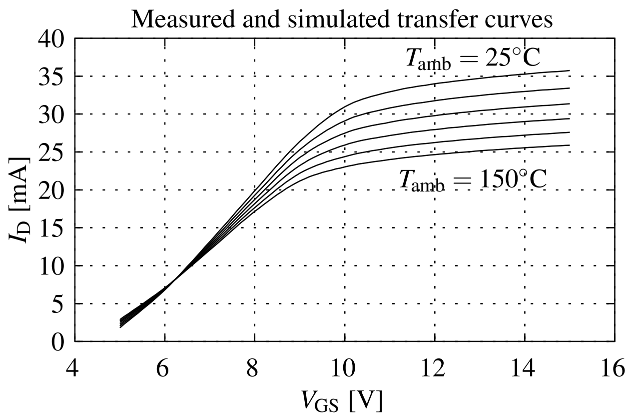

Fig. 6. Measured and simulated iso-thermal transfer curves using the TOPAS model at 25 °C…150 °C at $V_{\mathrm{DS}} = 9$ V. Simulation and measurement curves are identical.

B. CW verification

For cw verification simulated output characteristics have been compared to measurements at two different temperatures for a 7×100 μm LDMOS device. Fig. 7 shows that agreement for an ambient temperature of 25 $^\circ$ C, fig. 8 for an ambient temperature of 125 $^\circ$ C. Again, no differences between simulation and measurement can be obtained.

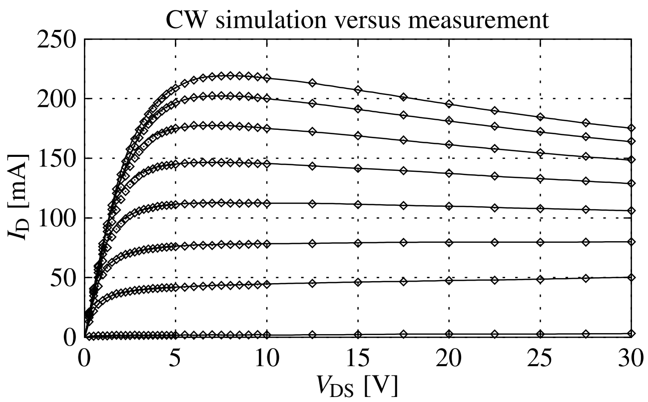

Fig. 7. Simulated and measured cw IV curves at 25 °C ambient temperature.

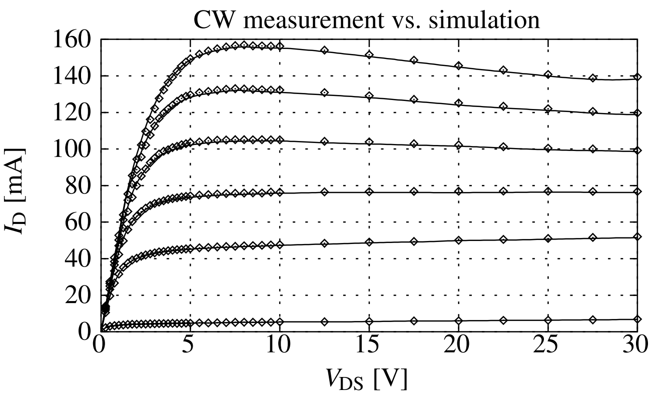

Fig. 8. Simulated and measured cw IV curves at 125 °C.

V. Conclusion

We presented a method of describing temperature dependent effects in transistor devices based on 3 dimensional spline functions $I_D(V_{GS}, V_{DS}, T)$. In opposite to many other equation based models our method allows a high precise description of non-linear temperature effects and can easily be implemented in any table based non-linear transistor model.

VI. Acknowledgement

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References

[1] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, “A New Dynamic Electro-Thermal Nonlinear Model For Silicon RF LDMOS FETs,” *IEEE Trans. Microwave Theory Tech.*, vol. 1, 1999.

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