

Extraction and Modeling Methods for FET Devices

R. Follmann, J. Borkes, P. Waldow, and I. Wolff

There are many ways of modeling field effect transistor (FET) devices. Physics-based models do not require any kind of measurements. They are completely based on the physics of the FET and simulate its behavior solving semiconductor equations for different geometries and doping profiles. Although these models are very flexible, they have not been useful to circuit design engineers because of their huge amount of computing time. The most common way in modeling FETs is the use of an equivalent circuit. The elements of the circuit are extracted using different kinds of measurements and afterwards described using either mathematical equations or look up tables. Both, equations and tables must allow interpolation between non-measured DC values.

This article describes an efficient method for FET modeling that requires a minimum number of measurements, namely only a set of small signal scattering parameters at different bias points. The proposed method is based on spline functions, takes into account thermal and noise effects, allows a scaling of different FET device geometries, and is available in commercial CAD software like Agilent's Series IV or ADS.

Equivalent Circuits

The equivalent circuit of a FET can be divided into two parts: constant and bias independent extrinsic elements and a bias dependent intrinsic part. Each element has a physical meaning. The extrinsic elements, for example, describe pad capacitances or resistivity of the transistor lines whereby the intrinsic charge zone of the FET is represented by the gate-source and gate-drain capacitances (Figure 1).

We propose an equivalent circuit [1] based on the well known 15 element circuitry [2,3]. Some changes (Figure 1), however, are required for the nonlinear modeling:

- All intrinsic elements are extracted bias dependent (both voltages)
- The current source I_{DS} is replaced by measured IV -curves $I_{DS}(V_{GS}, V_{DS})$

- Two Schottky diodes, which can be determined from the measured scattering parameters, describe its compression behavior
- The intrinsic conductance g is calculated by optimizing small signal scattering parameters at each bias point. All intrinsic elements depend on two bias voltages V_{GS} and V_{DS} .

The determination procedure of the extrinsic elements is well known. Using so called cold-scattering parameter measurements with $V_{DS} = 0V$, $V_{GS} < V_p$, and $V_{GS} \gg 0V$, whereby V_p is the pinch-off voltage of the device, R_S can for example be calculated as

$$R_S = \text{Re}\{z_{12}(f)\}. \quad (1)$$

The extraction of the extrinsic elements should not depend on the frequency f . In most cases, the extrinsic elements can also be determined through an optimization process comparing measured and simulated scattering parameters. In that case, varying intrinsic elements with varying extrinsic ones must be taken into account. The determination of the intrinsic elements is a bit more complicated, as can be seen in the equation for the extraction of the intrinsic capacitance

$$c_{GS}(V_{GS}, V_{DS}) = \sum_{f=f_1}^{f_2} \frac{1}{\omega} \left(\frac{\text{Im}\{y_{11}(V_{GS}, V_{DS})\}}{+\text{Im}\{y_{12}(V_{GS}, V_{DS})\}} \right) / (n_{f_2} - n_{f_1}). \quad (2)$$

Here, the median over a frequency range ($f_1 \dots f_2$) for n measured frequency points must be calculated. Figure 2 shows a typical example of the intrinsic gate-source capacitance in dependence of both V_{GS} and V_{DS} .

Many FET models show two main problems:

- dc simulation and intrinsic output conductance G_{DS} cannot be fit simultaneously for high frequencies [4]
- Determining a charge of a capacitance, which depends on two bias voltages, by a partial integration introduces new elements (transcapacitances) to the small signal equivalent circuit [4,5], to pre-

serve the consistence between small and large signal equivalent circuit.

The first problem can be solved using a topology shown in Figure 1, blocking capacitor C in series with bias dependent new output conductance $g(V_{GS}, V_{DS})$. A general solution for the second problem is given as follows.

Large Signal Modeling

For harmonic balance simulation purposes, the charge of each nonlinear capacitance must be calculated:

$$Q_1(v_1) = \int_0^{v_1} C(\tilde{v}_1) d\tilde{v}_1. \quad (3)$$

However the charge of a capacitance depending on two voltages is a function of the integration path

$$Q_2(v_1, v_2) = \int_0^{v_1} C(\tilde{v}_1, v_2) d\tilde{v}_1 + Q_1(v_2). \quad (4)$$

Therefore, a significant discrepancy between small and large signal models for low input power can often be noticed. For low input power, the large signal model must turn into the small signal model [4]. One way to solve this problem is to develop the voltage-dependent capacitance into a series

$$C(V_1, V_2) = \sum_{i=0}^n c_i(V_1) \cdot T_i(V_2), \quad (5)$$

where $c_i(V_1)$ and $T_i(V_2)$ can be integrated separately. This results in many additional steps of calculation and further inaccuracy.

An easier way to integrate a capacitance depending on two bias voltages into a large signal circuit simulator is to transform a charge source into its equivalent current source. The whole charge Q_G under the FET gate can be divided into two parts: a gate-source part Q_{GS} and a gate-drain part Q_{GD} . The large signal current of the gate-source part of the charge, for example, can then be calculated using (4):

$$i_{GS} = \frac{\partial Q_{GS}(v_{GS}, v_{DS})}{\partial t} = C'_{GS}(v_{GS}, v_{DS}) \cdot \frac{\partial v_{GS}}{\partial t}. \quad (6)$$

Since there is no dc current through a capacitance, C' is called a parametric capacitance. For the capacitance C'_{GS} , usually a Taylor approximation of the small signal capacitance c_{GS} is used.

Integration into CAD Software

In (6), the time derivative of a voltage dv/dt is needed, although most nonlinear frequency domain simulators do not give any access to these voltages or to any internal time step they use.

The time derivative of any voltage in a nonlinear frequency domain circuit simulation software (like HP-EEsofs series IV/ADS) can be calculated using the trick shown in Figure 3. Into the nonlinear node (Figure 3) flows a charge equal to $q = Cv$. The voltage v is that voltage, of which the time derivative is needed. During the harmonic balance analysis, the simulator calculates the current i_R through the resistor R as

$$i_R = \dot{q} = C \cdot \dot{v}. \quad (7)$$

The voltage across the terminal of the resistor and therefore the potential at the node, where the charge flows in, can be calculated as

$$v_R = i_R R = CR \cdot \dot{v}. \quad (8)$$

Many experiments with the harmonic balance engine of HP-EEsofs series IV/ADS have shown that values of $R = 100 \Omega$ and $C = 1e-16$ F are well suited for any harmonic balance calculation case. In order to simulate even dispersion effects, a value for C can be set in the μF area. In our model, one of these constructions is used for every nonlinear capacitance (Figure 1). To check, whether that implementation into a harmonic balance simulator is correct or not, small signal simulation of scattering parameters must be compared to scattering parameters that have been calculated using a large signal test bench with very low (-30 dBm) input power. In Figure 4, this verification can be seen for an $N = 4$ finger $W_t = 50 \mu\text{m}$ HEMT for the scattering parameter s_{21} . For very low input power, both the small signal and the large signal case result in identical scattering parameter simulation. For higher input power (0 dBm), the compression behavior of the device can be seen in the large signal simulation case. All other scattering parameters must show the same agreement, if the implementation is consistent.

The values of the intrinsic elements (see Figure 1, for c_{GS} example) should be described either as mathematical functions or using spline functions. The advantage of spline functions is that no equation coefficients have to be calculated, whereby as a drawback measurements have to be very accurate. Both mathematical description and spline functions must take care for a smooth extrapolation outside the measured region for harmonic balance calculation purposes. This is also true for any exponential function. These functions should be linearized for large arguments. For many CAD software packages, the element descriptions must be transformed to the intrinsic transistor voltages. Neglecting the gate current this can be done using (9):

$$\begin{aligned} V_{gs} &= V_{gs} - I_{ds}(V_{gs}, V_{ds}) \cdot R_S \\ V_{ds} &= V_{ds} - I_{ds}(V_{gs}, V_{ds}) \cdot (R_D + R_S). \end{aligned} \quad (9)$$

Diode Currents

Gate-source and gate-drain diode (Figure 1) can be extracted using different methods. One method is to dc-measure both diode currents in parallel and solve both diode equations iteratively. Another method is to use the measured IV output characteristic at $V_{DS} = 0 V$ in order to get the diode current I_G in dependence of V_{GS} . In order to save extensive dc measurements and computing time in solving diode equations, even small signal scattering parameters can be used for calculation of diode saturation current I_s and ideality factor n :

$$-\text{Re}\{y_{-12}\} = \frac{\partial I_D}{\partial U_{GD}} = \frac{I_s}{nV_t} \exp\left(\frac{U_{GD}}{nV_t}\right). \quad (10)$$

It can be shown that the error using scattering parameters for calculating diode currents is much less than the one using dc values and solving an equation system iteratively. Equation (10) can simply be solved using the method of linear regression.

Scaling, Temperature, and Noise

In most approaches, simple scaling functions are proposed in terms of doubling the transistor size is equivalent to double the output current and the intrinsic capacitances and halving the resistances. Our approach [6,7] measures and extracts the devices out of a matrix of transistors with varying numbers of gate fingers and different gate finger widths. From the scaling calculation, we take a cross of devices consisting of one line with constant number N of gate fingers and another line of constant gate finger width W_t . The intersection point of the two lines represents the reference device. Scaling the extrinsic elements is a simple procedure. Only the relationship between two bias independent elements has to be taken into account. But all intrinsic elements of a FET device depend on two voltages. Therefore, the usually used equation

$$c_{\text{old}} = \frac{\text{device area of new device}}{\text{device area of reference device}} \quad (11)$$

is not as accurate as our proposed equation (12) for calculating scaling coefficients c for the intrinsic elements

$$c_{\text{new}} = \frac{\sum_{V_{GS}, V_{DS}} \frac{E_{\text{ref}}(V_{GS}, V_{DS})}{E_{\text{scal}}(V_{GS}, V_{DS})}}{n_{V_{GS}, V_{DS}}}. \quad (12)$$

In (12), E_{ref} is the reference grid for the reference device, E_{scal} is the grid of the device, to that the reference device should be scaled and n is the number of bias points taken into account for the calculation of the scaling coefficients. The scaling coefficient for the reference device is scaling with N as well as scaling with W_t

$$S(N_{\text{ref}}) = S(W_{t,\text{ref}}) = 1. \quad (13)$$

In a first approximation, all scaling coefficients are interpolated using linear functions, whereby a is the slope and b the y-axis interception point of the straight line

$$S_j(x) = a_{jk} \cdot x + b_{jk}, \quad (14)$$

where x stands for either N or W_t . The overall scaling function for the intrinsic elements can be superposed

$$S_i(N, W) = S_i(N) \cdot S_i(W). \quad (15)$$

These functions can simply be expanded and are therefore suitable for any kind of simulation software and any kind of nonlinear model. The proposed theory can also be used for calculating temperature dependence of FET devices. Thus, nonintrinsic element grids for devices with different chip sizes are scaled, but dc output characteristics of the same device at different temperatures. Neglecting the temperature dependence of the capacitances [8], the temperature dependence of a FET can be expressed taking into account only dc characteristics at different temperatures and temperature variation of the resistances. With rising temperature, the I_{DS} current drops. For very high and very low temperatures, saturation effects can be seen. In a first approach, the temperature behavior of the output characteristics is simulated using (16)

$$S_{1/I_{DS}}(T) = \begin{cases} a_{1T} \cdot T + b_{1T} & \text{for } T < T_1 \\ a_{2T} \cdot T + b_{2T} & \text{for } T_1 \leq T < T_2 \\ a_{3T} \cdot T + b_{3T} & \text{for } T \geq T_2 \end{cases} \quad (16)$$

$$R_i(T) = R_i(T_0) \cdot [\gamma_{Ri}(T - T_0) + 1] \quad (16)$$

where T_1 and T_2 limit the median temperature range from saturation effects of very low and very high temperatures.

For noise calculation, adapted noise equations [8] are used. For a conductance of a noise resistance (17)

$$g_R = \frac{\langle i_{th}^2 \rangle}{4kT_0 \Delta f} \cdot \frac{T_{\text{sim}}}{T_0} \quad (17)$$

is used. The channel noise is modeled using (18)

$$g_{ids} = \left(\frac{1}{4kT_0} k_f \frac{I_{ds}^{a_f}}{f^b} + \frac{2}{3} \frac{T_0}{T_{\text{sim}}} \frac{\partial I_{ds}}{\partial V_{gs}} \right) \cdot \frac{T_{\text{sim}}}{T_0}, \quad (18)$$

where T_{sim} is the temperature for which the noise parameter should be calculated, T_0 is the actual temperature, k_f and a_f are noise coefficients, and b is the frequency exponent.

Verifications

The model has been verified on various MESFETs and HEMTs and was found to work very well within complex circuits containing more than one FET. In the meantime, a very complex Tx/Rx module has been successfully realized just using one scaleable transistor simulation file following the proposed approach. To demonstrate the models applicability to a four-finger 50 μm gate width HEMT (T420), the simulations of dc curves, small signal S -parameters, and a frequency-times-five multiplier are compared to measurements. In addition, an error grid containing the frequency-average complex difference between small signal S -parameter measurement and simulation for each bias point is given. Figure 5 shows the IV -curves simulation in a perfect agreement to the measurement.

As shown in the S -parameter error grid (Figure 6), the simulation of small signal S -parameters is in very good agreement to the measurement even for a large range of bias points, so that the reader will get a feeling of the small signal models quality from the total error grid. The average error is less than 5%. For very high positive voltages of V_{gs} , the error increases due to measurement and spline interpolating inaccuracies. But in comparison to the Curtice cubic model [9], the linear simulation still is very good.

In Figure 7, an up-scaling to an $N = 8$ finger $W_t = 75\mu\text{m}$ device of the same technology is shown in comparison to the measurement at a bias point of $V_{GS} = 0\text{ V}$ and $V_{DS} = 2\text{ V}$.

Figure 8 shows a down-scaling of the same device, this time at a bias point of $V_{GS} = 0\text{ V}$ and $V_{DS} = 0\text{ V}$.

Both simulations are in very good agreement to measurement, although the up-scaled device has twice the number of gate fingers and 1.5 times the gate finger width of the reference device. Similar good results can be achieved for any other bias condition.

For testing the quality of the whole model, even for generating harmonics, a frequency-times-five multiplier (Figure 9) was simulated and measured.

This extremely nonlinear circuit converts an input signal of 5 GHz to an output signal of 25 GHz using the 5th harmonic of the first transistor stage, which is driven into compression. The second stage serves as a buffer amplifier.

In Figure 10, the measurement of the 5th harmonic can be seen together with the simulation of the circuit using a Curtice cubic model [9] and the TOPAS [1, 6, 7] model using the calculation theory described previously. As can be seen, the simulation using the

TOPAS model is in good agreement to measurement, whereby the Curtice model has some seriously convergence problems in the power range between -5 and +5 dBm input power. Even simulation results are better using our approach. All other harmonics show similar excellent results.

Advantages

A state of the art method of nonlinear transistor modeling has been described using a minimum number of measurements. The proposed method has several advantages compared to other models:

- Small and large signal simulation results are identical for low input power
- Very good agreement between simulation and measurement for small signal, large signal and static simulation
- Valid for all bias points
- Scaling, temperature, and noise included
- Complete extraction and simulation within a very short time (<2 h)
- One set of parameters for any kind of circuit (amplifier, mixer, oscillator, switch, etc.).

References

- [1] R. Follmann, R. Tempel, T. Sporkmann, and I. Wolff, "A new spline based FET model for MESFETs and HEMTs," in *Proc. 27th European Microwave Conf. 2 (1997)*, no. 27, pp. 1360-1366.
- [2] G. Dambrine, A. Cappy, F. Helidore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151-1159, July 1988.
- [3] H. Fukui, "Determining of the basic parameters of a GaAs MESFET," *Bell System Tech. Journal*, vol. 58, no. 3, pp. 771-797, 1979.
- [4] D.E. Root and B. Hughes, "Principles of nonlinear active device modeling for circuit simulation," in *Proc. 32nd ARFTG Conf.*, Dec. 1988, pp. 3-26.
- [5] V. Calvo, A.D. Snider, and L.P. Dunleavy, "Resolving capacitor discrepancies between large and small signal FET models," *IEEE MTT-S Digest*, pp. 1251-1254, 1995.
- [6] R. Follmann, J. Herrmann, R. Tempel, T. Sporkmann, and I. Wolff, "New accurate scaling routines for any table/function based FET model including temperature and noise behaviour," in *Proc. EuMC 2 (1998)*, no. 28, pp. 97-101.
- [7] R. Follmann, J. Herrmann, R. Tempel, T. Sporkmann, I. Wolff, "New accurate scaling routines for any table/function based FET model including temperature and noise behaviour," in *Proc. GaAs 1 (1998)*, pp. 407-411.
- [8] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*. New York: McGraw-Hill, 1988.
- [9] W. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, no. 5, pp. 448-455, 1980.

Figure 1. Large signal equivalent circuit of a FET.

Figure 2. Typical shape of an intrinsic c_{GS} .

Figure 3. Trick to calculate dv/dt .

Figure 4. Comparison between small signal and large signal model.

Figure 5. dc output characteristics. Simulation versus measurement. $V_{GS} = -0.6 \text{ } 0.6 \text{ V}$ step 0.2 V .

Figure 6. Error grid for small signal simulation vs. Measurement.

Figure 7. Upscaled-device scattering parameters, simulated and measured.

Figure 8. Downscaled-device scattering parameters, simulated and measured.

Figure 9. Frequency times five multiplier.

Figure 10. Frequency times five multiplier, 3rd harmonic. Simulated and measured.

The method is based on spline functions, takes into account thermal and noise effects, allows scaling of different FET device geometries, and is available in commercial CAD software

These state-of-the-art procedures require a minimum number of measurements, i.e., only a set of small signal scattering parameters at different bias points

Consistent model implementation leads to identical simulation results for both small signal and large signal analysis with low input power

The model was verified on various MESFETs and HEMTs and was found to work very well within complex circuits containing more than one FET

R. Follmann, J. Borkes, P. Waldow, and I. Wolff are with the Institute für Mobil- und Satellitenfunktechnik (IMST) GmbH, Kamp-Lintfort, Germany